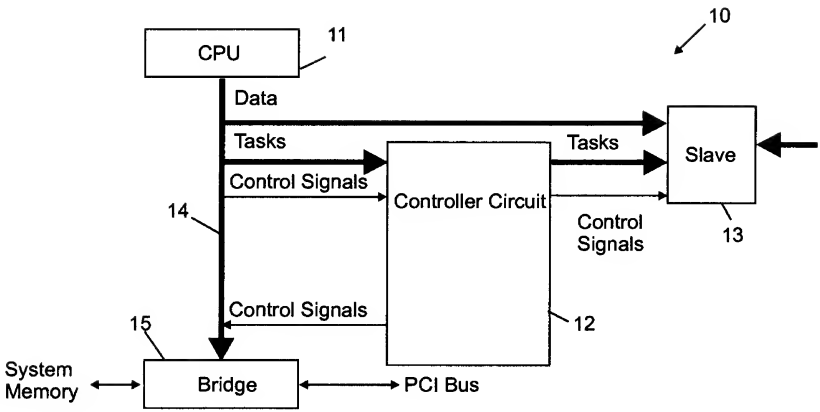


**FIG. 1 (Prior Art)**

| | | | Initial state | |
|---|---|---|---|---|
| CLEAR TASK Signal | ADD TASK Signal | TaskN-1 stored in AddressN-1 $V_{N-1}=1$ | TaskN stored in AddressN $V_N=1$ | Don't care AddressN+1 $V_{N+1}=0$ |
| 0 | 0 | No change $V_{N-1}=1$ | No change $V_N=1$ | No change $V_{N+1}=0$ |
| 0 | 1 | No change $V_{N-1}=1$ | No change $V_N=1$ | TaskN+1 (Task IN) $V_{N+1}=1$ |
| 1 | 0 | Task N $V_{N-1}=1$ | Invalid add $V_N=0$ | Don't care $V_{N+1}=0$ |
| 1 | 1 | Task N $V_{N-1}=1$ | TaskN+1 (Task IN) $V_N=1$ | Don't care $V_{N+1}=0$ |

1
2
3

Task N-1 is the oldest task

**FIG. 4**

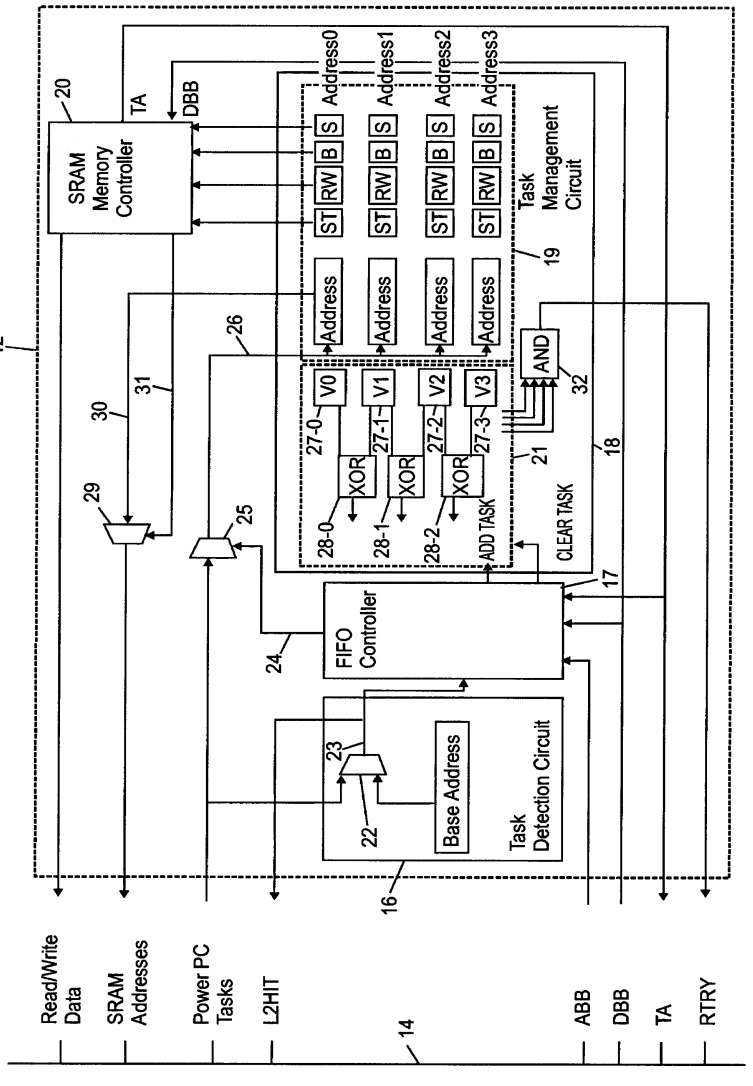
Read/Write Data
SRAM Addresses
Power PC Tasks
L2HIT
14
ABB
DBB
TA
RTRY
12
SRAM Memory Controller
20
TA
DBB
Address0
Address1
Address2
Address3
S
B
RW
ST
Address
Task Management Circuit
19
AND
32
V0
V1
V2
V3
27-0
27-1
27-2
27-3
XOR
28-0
28-1
28-2
ADD TASK
CLEAR TASK
21
18
17
26
30
31
29
25
24
FIFO Controller
23
22
Base Address
Task Detection Circuit
16

FIG. 2

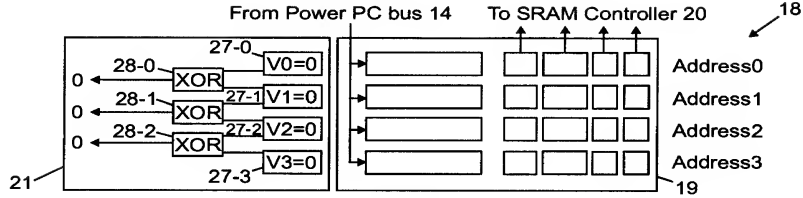


FIG. 3a

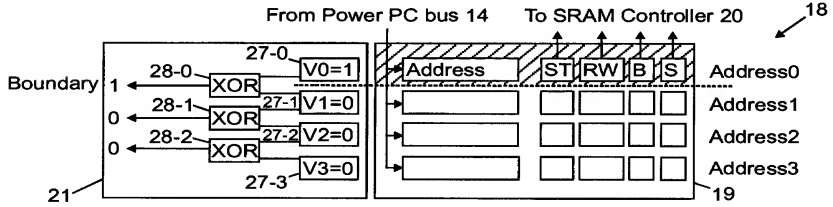


FIG. 3b

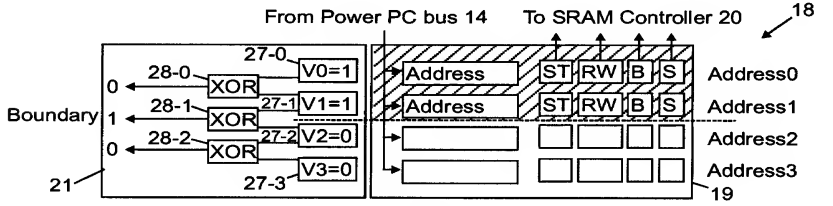


FIG. 3c

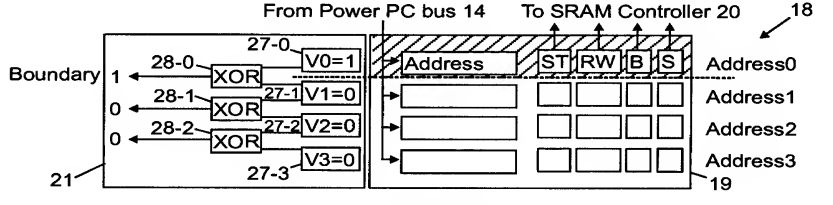


FIG. 3d

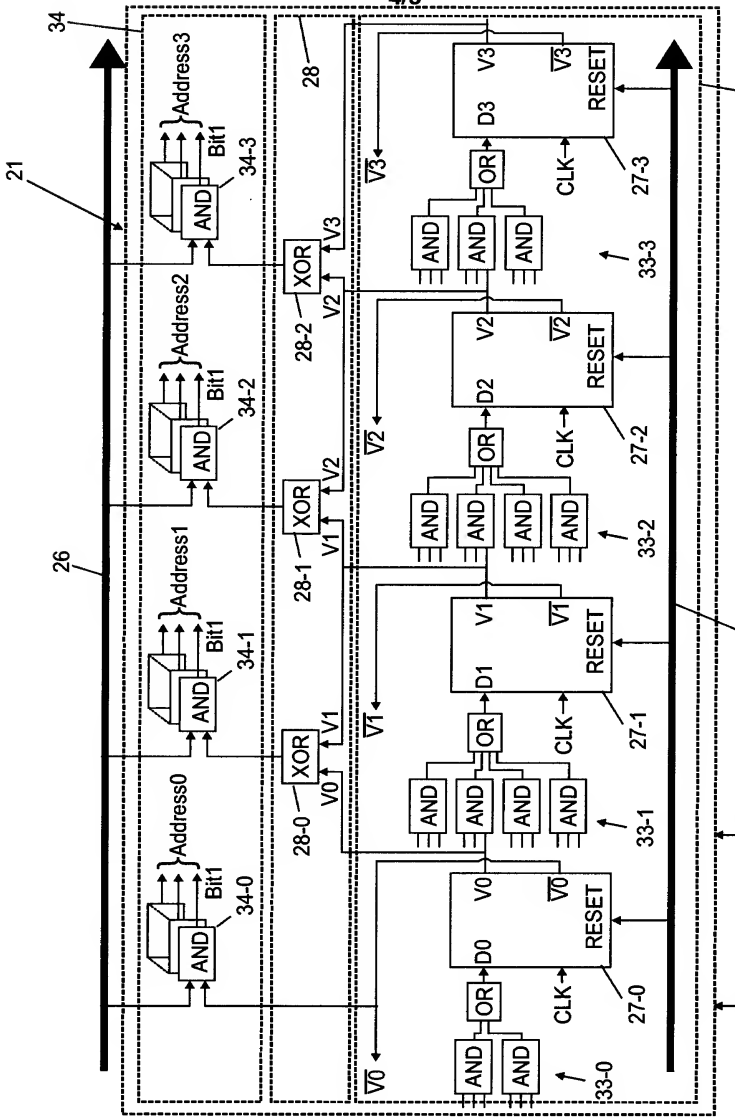
34
21
26
28
27
32
Address0
Address1
Address2
Address3
Bit1
AND
34-0
34-1
34-2
34-3
XOR
28-0
28-1
28-2
V0
V1
V2
V3
D0
D1
D2
D3
RESET
CLK
OR
27-0
27-1
27-2
27-3
33-0
33-1
33-2
33-3
ADD TASK
CLEAR TASK

FIG. 5

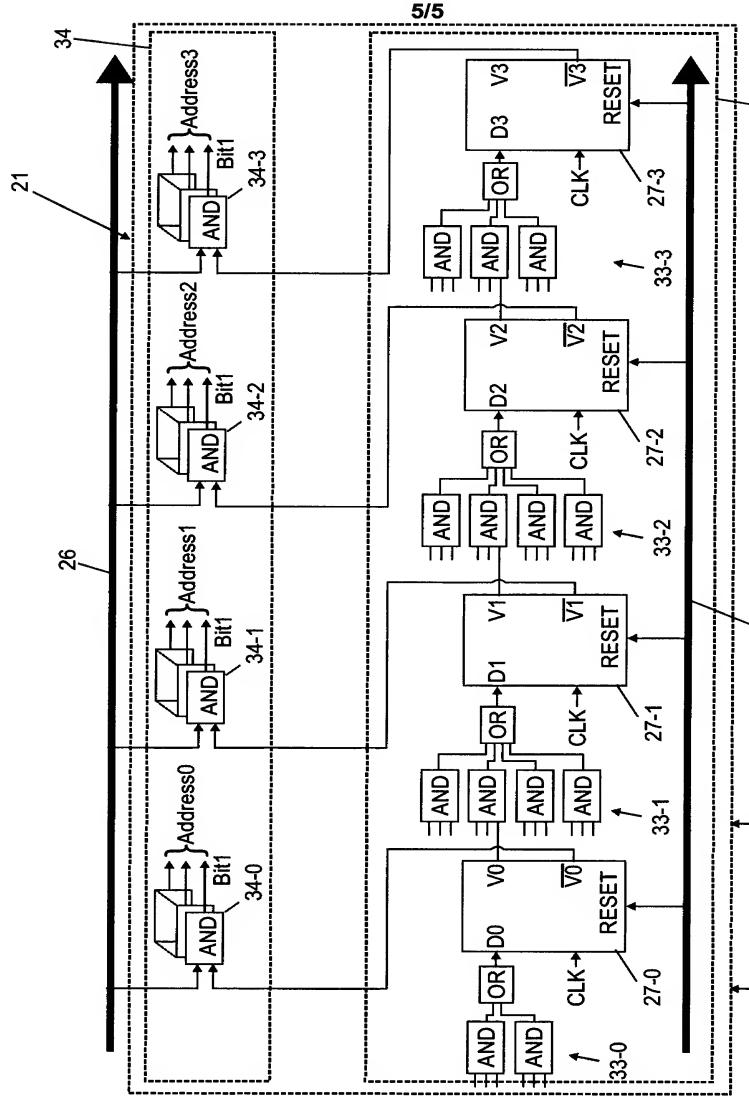
34
21
26
32
27
Address0
Address1
Address2
Address3
Bit1
AND
OR
CLK
RESET
D0
D1
D2
D3
V0
V1
V2
V3
34-0
34-1
34-2
34-3
27-0
27-1
27-2
27-3
33-0
33-1
33-2
33-3
ADD TASK
CLEAR TASK

FIG. 6